Report

Industry-Oriented Workshop on Cadence Virtuoso

1st September – 2nd September, 2026

Venue: GTU – School of Engineering and Technology, Academic Block 5, GTU Campus, Chandkheda, Ahmedabad

Coordinator: Prof. Gautam D. Makwana
Co-coordinator: Prof. Aayushi Garg

Introduction

The Industry-Oriented Workshop on **Cadence Virtuoso** was conducted to provide participants with practical exposure to **VLSI design methodology, CMOS circuit design, simulation and layout implementation** using the Cadence Virtuoso environment. The workshop combined fundamental concepts with hands-on laboratory sessions, enabling participants to understand the complete VLSI design flow from **schematic design and circuit simulation to physical layout**.

The workshop covered important aspects of VLSI and CMOS design, including **VLSI design methodology and flow, Cadence Virtuoso environment, MOS transistor concepts, CMOS inverter design, DC and transient simulation, switching characteristics, interconnect effects, CMOS combinational logic, layout design rules and the CMOS n-well process**.

The hands-on approach enabled participants to apply the concepts discussed during the technical sessions through schematic creation, circuit simulation and layout implementation. The workshop thereby provided an integrated understanding of the major stages involved in **CMOS VLSI design and semiconductor circuit development**.

Day 1: VLSI Design Methodology, Cadence Virtuoso and CMOS Circuit Design

Date: 01-09-2026 to 10-07-2026

Session Details

Dr. Madhuri Bhavsar, Director adressing the participants

Participants

Prof. Gautam Makwana teaching ASIC Design Flow

Mr.Apurv simulating IV curves of MOSFET

Topics covered

Objective:

- To provide practical exposure to the Cadence Virtuoso-based VLSI design flow.
- To familiarize participants with CMOS circuit design, simulation and layout implementation.
- To bridge theoretical concepts with practical circuit development.

Session Details:

- The workshop introduced VLSI design methodology, Cadence Virtuoso, PDK setup, Library Manager, cell views and MOS transistor concepts.
- Participants performed NMOS/PMOS schematic entry and CMOS inverter design, followed by DC simulation using ADE to study VTC and noise margins.
- Further sessions covered switching characteristics, propagation delay, rise/fall times, interconnect effects and transient simulation.
- Participants also worked on CMOS combinational logic, including NAND, NOR, complex gates and transmission gates.
- The workshop concluded with CMOS n-well process, layout design rules and practical CMOS inverter layout using the Cadence Virtuoso Layout Editor.

Topics Covered:

- VLSI design methodology and flow
- Cadence Virtuoso and MOS transistor concepts
- CMOS inverter design and DC/transient simulation
- Switching characteristics and interconnect effects
- CMOS combinational logic
- CMOS n-well process and layout design rules

Ms. Nidhi teaching about MOSFETS

Mr. Jiten showing simulations of capacitance in MOSFET

Tools Used:

- Cadence Virtuoso
- Analog Design Environment (ADE)
- PDK and Library Manager
- Cadence Virtuoso Layout Editor
- CMOS n-well process

Learning Outcome:

- Gained practical understanding of the CMOS VLSI design flow.
- Developed hands-on experience in schematic creation, simulation and layout.
- Understood switching behaviour, CMOS logic and layout design principles.
- Developed skills relevant to VLSI and semiconductor circuit development..

Conclusion

The workshop successfully provided participants with practical knowledge of the **Cadence Virtuoso-based VLSI design flow**, beginning with VLSI design methodology and fundamental CMOS concepts and progressing through schematic entry, circuit simulation, CMOS combinational logic and physical layout implementation.

The two-day workshop combined **technical sessions and hands-on laboratory exercises**, providing participants with exposure to Cadence Virtuoso, DC and transient simulation, switching behaviour, interconnect effects, CMOS logic circuits, layout design rules and the CMOS n-well process. The practical approach helped participants develop an integrated understanding of CMOS VLSI design and provided a foundation for further work in **VLSI, semiconductor design and electronic design automation (EDA)**.

GUJARAT TECHNOLOGICAL UNIVERSITY

SCHOOL OF ENGINEERING AND TECHNOLOGY

(E.C) (A.Y. 2026-27) (Semester 5)

Attendance sheet

VLSI WORKSHOP : 01 /09/2026 - 02/09/2026

Sr. No.	Enrollment No.	Name of Student	01 /09/2026	02/09/2026
1	241370111001	PRAJAPATI AVANI HITENDRABHAI	Avani	Avani
2	241370111002	BHALODIYA YASHVIBEN SHANTILAL	YSV	YSV
3	241370111003	BRAHMANIYA HARNISH LALJIBHAI		
4	241370111004	DARSHKUMAR DOBARIYA		
5	241370111005	DUBEY PRABHA SANTOSHKUMAR		
6	241370111006	DUTT RISHEEKA NITESHBHAI		
7	241370111007	FAPALE ISHWARI ANILBHAI		
8	241370111008	PRAJAPATI HELLY GOVINDBHAI		
9	241370111009	JAIN PRANAV MOHIT(ROBOCON)		
10	241370111010	KAMDAR KAAVYA KRITIN		
11	241370111012	KHUSHI PATEL		
12	241370111013	KRISHA MODI		
13	241370111014	DODIYA KRISHNARAJSINH HITESH		
14	241370111015	MAKWANA VIR SURESHBHAI		
15	241370111017	FAKIH MARIYA TAHER		
16	241370111018	MODI PRATHAM PANKAJ		
17	241370111019	BHAVSAR NISARG PRADIPKUMAR		
18	241370111020	PADARIYA KASHYAP NARESHBHAI		
19	241370111021	PANCHAL MIT RAJESHKUMAR		
20	241370111022	PATEL HARSHKUMAR SANJEEVKUMAR		
21	241370111023	PATEL KASHISH KHANJANKUMAR		
22	241370111024	PATEL LAV SAUMILKUMAR		
23	241370111025	PATEL MAHIR MANOJKUMAR		
24	241370111026	PATEL SARVA VISHNUKUMAR		
25	241370111027	PATEL SUCHI DILIPKUMAR		

			2/9	2/9
26	241370111028	PATEL VED JAYESHBHAI		
27	241370111029	PRAGADA NIDHI HITESHBHAI		
28	241370111030	PRAJAPATI HARSHKUMAR RAKESHKUMAR		
29	241370111031	RAJ YOGESHWARSINH UPENDRASINH		
30	241370111032	CHAUHAN RITIKA DILIPBHAI		
31	241370111033	ROHAN HITESH PURANIK		
32	241370111034	SUMESARA DHAIRYARAJ DINESHCHANDRA		
33	241370111035	MAJITHIA TANIA MAHESH		
34	241370111036	VOHERA MAHI PARESHKUMAR		
35	241370111038	AVROJIT BHATTACHARJEE		
36	241370111039	GOURAB BISWAS		
37	241370111040	MD. ALI IBNA TAWSIM		
38	241370111041	MITHUN KUMER DEV		
39	241370111042	NILOY KISHOR ROY		
40	241370111043	PREETAM CHAKRABORTTY		
41	241370111044	RATUL MOHORY NIL		
42	251373111001	BAROT NEET ALKESHBHAI		
43	251373111002	PANCHAL SUJAL RAMESHBHAI		
		No. of Present		
		No. of Absent		
		Total (No. of Student)		

2026MEVLSI06 GAURAV MAKWANA

2026MEVLSI02 Vicky Singh

2026MEVLSI01 Moktar Abdourahman Moussa

2026MEVLSI04 Abhimanyu

2026MEVLSI06 Moyasser

2026MEVLSI03 Vivek Mistry

2026MEVLSI05 Brajendra Kr.