Report

Orientation and Kick-off Program

ChipIN Extension Centre (CoE – VLSI Design)

6th August 2026 to 7th August 2026

Venue: B0 Hall, Gujarat Technological University

In collaboration with GSEM & C-DAC

Coordinated by:
Prof. Gautam D. Makwana, Asso. Prof. GTU-SET

About the Program

The Orientation and Kick-off Program of the ChipIN Extension Centre (CoE – VLSI Design) was organized by Gujarat Technological University (GTU) in collaboration with the Gujarat State Electronics Mission (GSEM) and the Centre for Development of Advanced Computing (C-DAC). The program was conducted on 6th and 7th August 2026 at the GTU Campus, Chandkheda, Ahmedabad.

This initiative is part of the national effort under the India Semiconductor Mission (ISM), aimed at strengthening the semiconductor ecosystem in India through academic enablement, infrastructure development, and skilled manpower generation. The establishment of the ChipIN Extension Centre at GTU represents a strategic step toward providing institutions with access to advanced semiconductor design infrastructure, including Electronic Design Automation (EDA) tools and High-Performance Computing (HPC) facilities.

The program witnessed active participation from academic institutions across Gujarat. A total of 65 participants from 32 institutes attended the orientation, including Principal Investigators (PIs), Co-Principal Investigators (Co-PIs), faculty members, and researchers. This participation reflects strong institutional interest and commitment toward semiconductor education and research.

The primary objective of the program was to introduce the framework, objectives, and implementation strategy of the ChipIN initiative, along with facilitating institutional onboarding. It also aimed to provide exposure to industry-standard tools such as Cadence and Synopsys, and to familiarize participants with HPC-based semiconductor design workflows.

Registration and Inauguration

Light Lamping and Saraswati Vandana

Felicitation of Smt. P. Bharati,Secretary-DST by former Dr. Rajul Gajjar, VC-GTU

Felicitation of Ms. Neha Kumari, Mission Director-GSEM by Dr. Vaibhav Bhattr, VC-GTU

Felicitation of Dr. N. Subramanian, Executive Director, SETS by Dr Madhuri Bhavsar Director GTU-SET

- The Orientation and Kick-off Program of the ChipIN Extension Centre (CoE – VLSI Design) commenced with the registration of participants, followed by the formal inaugural session on 6th August 2026 at Gujarat Technological University (GTU), Ahmedabad..
- The inaugural session began with Saraswati Vandana, followed by the GTU anthem, setting a formal and academic tone for the program.
- The session was attended by distinguished dignitaries from academia, government, and industry, including Dr. Rajul Gajjar, Former Vice-Chancellor, GTU; Dr. Vaibhav Bhatt, In-charge Vice-Chancellor, GTU; Smt. P. Bharati, Secretary, Department of Science and Technology (DST), Government of Gujarat; Ms. Neha Kumari, Mission Director, GSEM; Dr. Rajat Moona, Director, IIT Gandhinagar; Dr. N. Subramanian, Executive Director, SETS, Chennai; Shri Senthil Kumar R., C-DAC Bengaluru; and Dr. K. N. Kher, Registrar, GTU.
- The program was formally welcomed by Dr. Madhuri Bhavsar, Director, GTU School of Engineering and Technology, who emphasized the importance of developing a strong semiconductor ecosystem through academic participation and infrastructure support.
- Shri Senthil Kumar R. presented an overview of C-DAC's activities and its contributions toward high-performance computing and semiconductor research.
- Dr. Vaibhav Bhatt highlighted GTU's role in the India Semiconductor Mission and announced that the ChipIN Extension Centre would provide GTU-affiliated institutes with access to industry-standard Electronic

Welcome address by Dr Madhuri Bhavsar, Director-GTU SET

Dr. Vaibhav Bhatt, VC-GTU, addressing the participants

Participants address by Smt. P. Bharati

Vote of Thanks by Dr. R.A. Thakker

Design Automation (EDA) tools such as Cadence and Synopsys.

- Further, Dr. N. Subramanian discussed the growing semiconductor ecosystem in India and the importance of skill development and research.
- Dr. Rajat Moona highlighted national initiatives such as SAMARTH and appreciated the collaborative efforts between GTU and IIT Gandhinagar.
- Smt. P. Bharati encouraged faculty members and Principal Investigators to actively utilize the opportunities provided under the ChipIN initiative for institutional and research advancement.
- The inaugural session outlined the key objectives of the ChipIN initiative, including institutional onboarding, awareness of High Performance Computing (HPC) resources, and strengthening collaboration among GTU, C-DAC, GSEM, IIT Gandhinagar, SETS, and affiliated institutions.
- The session concluded with a vote of thanks delivered by Dr. R. A. Thakker, Advisor, CoE-AI and Director, Research and Development Cell (RDC), GTU, who expressed gratitude to the distinguished dignitaries, organizing team, and participants for their valuable contributions to the successful conduct of the inaugural program.
- The ceremony formally concluded with the national song followed by the national anthem, marking the end of the inaugural session on a respectful and patriotic note.
- Overall, the inaugural session effectively established the vision and direction of the ChipIN Extension Centre, setting a strong foundation for the technical deliberations and collaborative engagements scheduled in the subsequent sessions of the program.

Day 1: Orientation and ChipIN Onboarding Sessions

Date: 06-08-2026

Session Details

Introduction to High Performance Computing

Participants

Testimonials from CDAC

Topics covered

Objective:

- To introduce the ChipIN initiative and its role in the India Semiconductor Mission.
- To provide a structured understanding of institutional onboarding and shared semiconductor infrastructure.
- To create awareness about High Performance Computing (HPC) systems for semiconductor design and simulation.
- To familiarize participants with national-level resources, EDA access frameworks, and collaborative research opportunities.

Session Details:

- The day began with the inaugural session followed by a technical lecture by Shri Senthil Kumar R., who presented an overview of C-DAC and its contributions to India's indigenous technology development.
- The session provided detailed insights into High Performance Computing (HPC) systems such as PARAM series supercomputers, explaining their architecture based on distributed computing, parallel processing, and high-speed interconnect networks. The relevance of HPC in semiconductor workflows was emphasized, particularly for computationally intensive tasks such as RTL simulation, large-scale verification, physical design analysis, and TCAD-based device modeling.
- The session also highlighted C-DAC's role in enabling national missions through development of advanced computing platforms and semiconductor design support infrastructure.
- This was followed by testimonial

Overview of C-DAC by Shri Senthil Kumar

Felicitation of Shri. Senthil Kumar by Dr. R.A. Thakker

Testimonies from C-DAC

Participants

presentations from C2S (Chips to Startup) participating institutions.

- The institutes shared practical experiences related to adoption of semiconductor design ecosystems in academia.
- Key discussions included challenges such as limited access to licensed EDA tools, high computational requirements for simulation and verification, and the need for skilled manpower in RTL design, verification, and physical design.
- Institutes also discussed implementation of FPGA-based prototyping platforms, lab setup strategies, and efforts to align academic curriculum with industry-standard semiconductor design flows.
- These testimonials provided a realistic understanding of the current academic landscape and the necessity of centralized initiatives like ChipIN.
- The final session of the day was conducted by Shri Gokulatheerthan M., focusing on **High Performance Computing (HPC) resources and their application in semiconductor design workflows**.
- The session provided technical insights into HPC cluster architecture, including compute nodes, storage systems, and network interconnects.
- It also covered job scheduling mechanisms, parallel execution models, and resource allocation strategies.
- The application of HPC in semiconductor design was discussed in detail, including its role in simulation acceleration, timing analysis, design rule checking (DRC), layout versus schematic (LVS) verification, and large-scale data processing required for device and circuit modeling.
- The session highlighted how HPC infrastructure significantly reduces computation time and enables complex design iterations in modern VLSI workflows.
- Each session concluded with an

Application of HPC in semiconductor Design

Anchoring by Dr. K. R. Borisagar

Interaction with Participants

Group Photo with dignitaries

interactive discussion, where participants' queries were addressed, ensuring clarity of concepts and effective knowledge transfer.

Topics Covered:

- C-DAC and its role in HPC and semiconductor ecosystem development.
- ChipIN platform architecture and institutional onboarding framework.
- Challenges in semiconductor education and infrastructure adoption (C2S insights).
- HPC architecture: parallel computing, cluster design, and job scheduling.
- Application of HPC in RTL simulation, verification, physical design, and TCAD modeling.

Tools/Technology Discussed:

- Electronic Design Automation (EDA) Tools (Cadence, Synopsys – conceptual exposure).
- High Performance Computing (HPC) Clusters.
- Job Scheduling and Parallel Processing Systems.
- FPGA-based Prototyping Platforms (conceptual discussion).
- Semiconductor Design and Verification Workflows.

Learning Outcome:

- Developed a clear understanding of the ChipIN ecosystem and institutional onboarding process.
- Gained technical knowledge of HPC systems and their role in semiconductor design acceleration.
- Understood practical challenges in implementing VLSI design infrastructure in academic institutions.

Day 2: Advanced Semiconductor Systems and Tape-Out Practices

Date: 07-08-2026

Session Details

Mr. Arun Nath on VEGA RISC-V Processor

Felicitation of Mr. Arun Nath By Dr. S.K. Hadia

Dr. H.S. Jatana on Semiconductor Processes

Felicitation of Dr. H.S. Jatana by Dr Madhuri Bhavsar

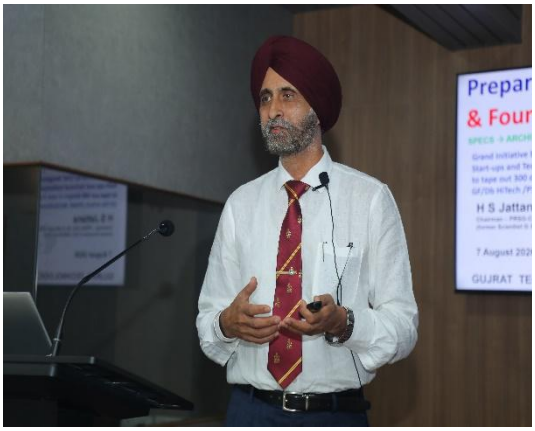
Topics covered

Objective:

- To provide advanced insights into processor design, semiconductor fabrication, and system-level integration.
- To introduce indigenous processor ecosystems and SoC development methodologies.
- To familiarize participants with tape-out procedures and foundry-level practices.
- To expose participants to embedded systems and IoT-based product development.

Session Details:

- The day commenced with a technical session by Shri Arun S. Nath on the **VEGA RISC-V Processor Ecosystem**, where participants were introduced to indigenous processor design using open-standard RISC-V architecture.
- The session covered instruction set architecture (ISA), processor pipeline design, and customization of cores for application-specific requirements.
- It also included discussion on System-on-Chip (SoC) integration, hardware accelerator design, and FPGA-based prototyping, highlighting the transition from design to real-world deployment.
- This was followed by a session by Dr. H. S. Jatana on **"Preparing for First Silicon: Tape-Out and Foundry Best Practices"**, which provided detailed technical insights into semiconductor fabrication readiness.
- The session covered critical pre-tape-out stages including design rule checking (DRC), layout versus schematic (LVS), static timing analysis, and power integrity verification.
- It also emphasized process variation, yield optimization, reliability considerations, and adherence to foundry design kits (PDKs) for successful silicon fabrication.
- The next session was delivered by Shri Shamjith K. V., focusing on **IoT products and system-level solutions**.



Interaction of Dr. Jatana with participants

Shri Shamjith K. V. session on IoT products and system-level solutions.

Felicitation of Shri Shamjith K.V. by Dr. Gautam Makwana

- The session provided a comprehensive understanding of embedded system architecture, including microcontroller/microprocessor interfacing, sensor integration, and real-time data acquisition.
- Communication protocols such as UART, SPI, and I2C were discussed along with wireless connectivity in IoT ecosystems. The session emphasized hardware-software co-design, firmware development, and system optimization for scalable and power-efficient IoT applications.
- Each session concluded with an interactive discussion, where participants' queries were addressed, ensuring clarity of concepts and effective knowledge transfer.

Topics Covered:

- RISC-V processor architecture and SoC design.
- FPGA-based prototyping and hardware acceleration.
- Semiconductor fabrication process, tape-out flow, and foundry practices.
- Embedded systems and IoT architecture.
- Communication protocols and system-level integration

Tools Used:

- RISC-V Processor Ecosystem
- FPGA Development Platforms
- Semiconductor Verification Tools (DRC, LVS, STA).
- Foundry Design Kits (PDKs)
- Embedded Systems and IoT Development Frameworks.

Learning Outcome:

- Gained integrated understanding of semiconductor design flow, processor architecture, fabrication readiness, and system-level application development.

Closing Ceremony:

Felicitation of Shri Abey Jacob by Dr Madhuri Bhavsar and Dr. R.A.Thakkar

Feedback from Shri Abey Jacob

Participants Feedback

Dr Madhuri Bhavsar addressing the participants

- The successful completion of the two-day Orientation and Kick-off Program was marked by a formal closing session held at the end of Day 2.
- The session began with the acknowledging the presence of Shri Abey Jacob, Shri Abey Jacob, Senior Scientist, C-DAC Bengaluru whose support and contribution were instrumental in organizing the program.
- He was felicitated as a token of appreciation for his valuable involvement by Dr. Madhuri Bhavsar and Dr. R.A. Thakker.
- Shri Abey Jacob shared his valuable feedback, emphasizing the importance of collaborative initiatives in strengthening the semiconductor ecosystem and promoting active participation from academic institutions.
- Feedback was subsequently collected from the participants to assess the effectiveness of the sessions, technical content, and overall organization of the program.
- Participants expressed positive feedback and conveyed their interest in having more such programs in the future, emphasizing the need for continued initiatives to enhance practical knowledge and industry exposure in the semiconductor domain.
- Dr. Madhuri Bhavsar, Director, GTU-SET, expressed her sincere gratitude to all the industry experts, participants, and the organizing team.
- She also highlighted the existing skill gap in the electronics and semiconductor domain, emphasizing the need for such initiatives to equip students and professionals with industry-relevant knowledge and practical exposure.
- Dr. R. A. Thakker delivered the concluding remarks, appreciating the collaborative efforts of all stakeholders.
- He expressed special gratitude to Shri Abey Jacob for enabling this collaboration and further stated that such initiatives aim to fulfill the commitment of achieving **“one chip designed per institute”**, thereby strengthening the semiconductor

Concluding Remarks by Dr. R.A.Thakker

design ecosystem at the institutional level and there by contributing to India's Semiconductor Mission.

- The event concluded with a group photograph, marking the successful completion of the Orientation and Kick-off Program.
- Overall, the program successfully achieved its objectives by providing valuable technical insights and fostering collaborative learning in the semiconductor domain.

Group Photos