Report

Industry based Summer Internship (2 weeks)

on

RTL to GDS-II: From Silicon to Design

6th July 2026 to 17th July 2026

Coordinator: Prof. Gautam D. Makwana

Introduction

The two-week Summer Internship on "**From Digital Design to Silicon Chip: RTL to GDS-II**" was organized by the GTU School of Engineering and Technology in collaboration with eInfochips – An Arrow Company, Ahmedabad from 6th July 2026 to 17th July 2026 at the GTU Semiconductor Chip Design Laboratory supported by Chips2Startup, MeitY, New Delhi and ICICI Foundation.

Objective of the internship are to provide comprehensive exposure to the complete ASIC design flow, ranging from Register Transfer Level (RTL) design to GDS-II generation using industry-standard Electronic Design Automation (EDA) tools such as Cadence and Synopsys for the students of B.E. Electronics & Communication, 7th Semester of the GTU affiliated colleges, to bridge the gap between academic learning and industrial requirements through sessions and hands-on practices by renowned industrial experts.

The internship includes various process step of ASIC design flow such as modern semiconductor design methodologies including RTL design, Design for Testability (DFT), logic synthesis, physical design, verification, and sign-off analysis using Cadence and Synopsys EDA tools.

A total of 38 students from various GTU-affiliated engineering colleges across Gujarat participated in the internship. The institute-wise participation is presented in Table 1.

Table 1 Institute wise Participation

Name of Institute	Number of students
Vishwakarma Government Engineering College, Ahmedabad	15
L.D. College of Engineering, Ahmedabad	12
Government Engineering College, Rajkot	7
Government Engineering College, Gandhinagar	4

Registration and Inauguration

Felicitation of Mr. Rutvik Govindia

Felicitation of Ms. Chandni Patel

Dr. Madhuri Bhavsar, Director, GTU-SET welcoming participants and Industry Experts

Participants Interaction with Industry Experts

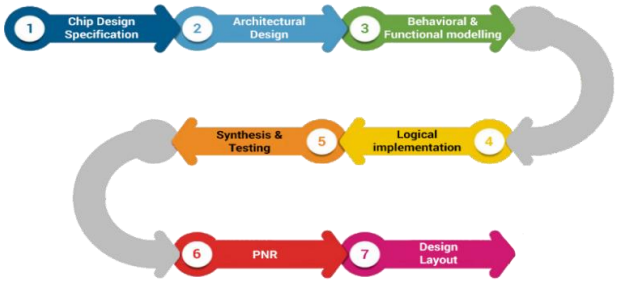
- The internship commenced with a brief inaugural session and participant registration.
- Each participant was provided with an internship kit consisting of a diary, pen, and folder to facilitate note-taking and documentation throughout the programme.
- The participants and industry experts, Mr. Rutvik Govindia and Ms. Chandni Patel were welcomed by Dr. Madhuri Bhavsar, Director, GTU School of Engineering and Technology, who also emphasized the growing importance of semiconductor technologies and the need for industry-oriented skill development to meet the demands of the rapidly expanding semiconductor ecosystem.
- The Director also appreciated the collaborative efforts of GTU and eInfochips – An Arrow Company in organizing an internship that combines academic knowledge with practical industrial exposure.
- Following the welcome address, Prof. Gautam D. Makwana, Internship Coordinator, introduced the objectives, structure, schedule, and expected learning outcomes of the internship, and encouraged the participants to actively engage in the technical sessions, laboratory activities, and industry interactions to strengthen their practical skills in VLSI and semiconductor chip design.
- The inaugural session concluded with the introduction of the industry experts from eInfochips - An Arrow Company, following which the first technical session on "ASIC Flow and Design for Testability Fundamentals and Scan Architecture" was delivered by Mr. Rutvik Govindiya marking the commencement of the internship programme

Week 1: Foundation of ASIC Design and RTL Implementation

Date: 06-07-2026 to 10-07-2026

Session Details

Introductory session on ASIC Design Flow



ASIC Design Flow

Participants understanding Foundational Terms

Hands on Practice sessions

Topics covered

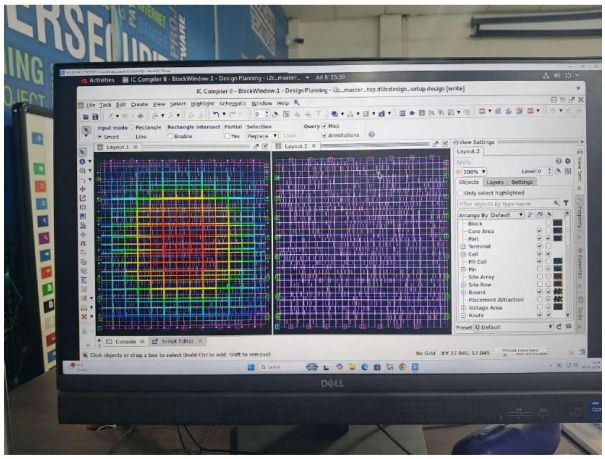
Objective:

- To introduce participants to the complete ASIC design flow and familiarize them with the various stages involved in semiconductor chip design from RTL to GDS-II.
- To provide a strong conceptual understanding of Design for Testability (DFT), scan architecture, ATPG, and fault simulation techniques used in modern VLSI design.
- To develop practical skills in RTL design and Verilog HDL programming through hands-on implementation of combinational and sequential digital circuits.
- To provide participants with exposure to industry-standard Synopsys EDA tools used for logic synthesis, physical design, simulation, and debugging.

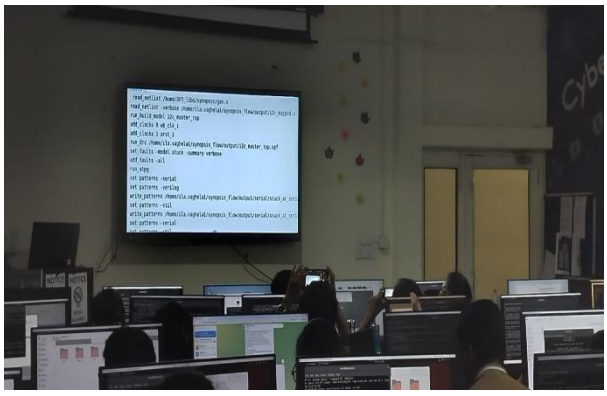
Session Details:

- The week commenced with an introduction to the complete ASIC design flow, where participants learned the various stages involved in transforming a digital specification into a fabricated integrated circuit. Mr. Rutvik Govindia introduced the concepts of ASIC design methodology and explained the significance of each design stage in semiconductor development.
- Mr. Rutvik Govindia and Ms. Chandni Patel conducted sessions on logic synthesis and semiconductor design methodologies, introducing RTL synthesis, technology mapping, timing analysis, and the semiconductor industry ecosystem.
- Participants gained practical exposure to physical design implementation.

Gate Level Schematic HDL Codes



Hands on sessions for Floorplan and placement



Hands on sessions for Routing

- Also included, floorplanning, placement, clock tree synthesis, routing, timing verification, and physical sign-off using Synopsys IC Compiler II during the laboratory sessions.
- Mr. Siddhesh Patil introduced Verilog HDL programming concepts and demonstrated structural, dataflow, and behavioural modelling techniques through hands-on implementation of digital circuits.
- The week concluded with sessions on sequential circuit design, finite state machine fundamentals, waveform analysis, and interactive hands-on exercises, followed by daily question-and-answer sessions with the industry experts.

Topics Covered:

- Complete ASIC design flow from RTL design to GDS-II generation.
- Design for Testability (DFT), Scan Architecture, Embedded Deterministic Test (EDT), ATPG, and fault simulation techniques.
- Logic synthesis, technology libraries, timing analysis, power optimization, and semiconductor industry workflow.
- Physical design concepts including floorplanning, placement, clock tree synthesis, routing, DRC, LVS, IR-drop analysis, and GDS-II generation.
- Verilog HDL programming, RTL modelling, combinational and sequential circuit design, simulation, and waveform debugging.

Tools Used:

- Synopsys Design Compiler (DC)
- Synopsys IC Compiler II (ICC2)
- Synopsys VCS Simulator
- Synopsys Verdi Debugger
- Verilog HDL

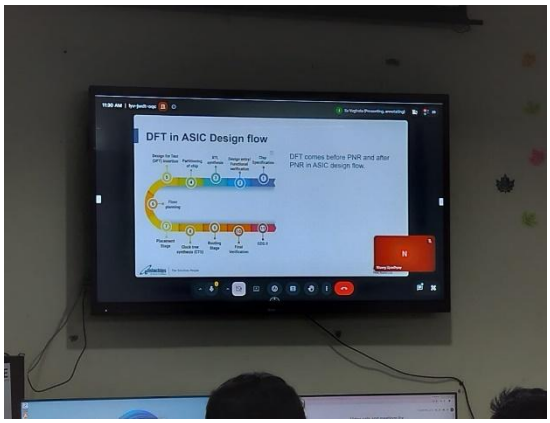
Learning Outcome:

- Developed a strong foundation in ASIC design, RTL design, Verilog HDL, and physical design.

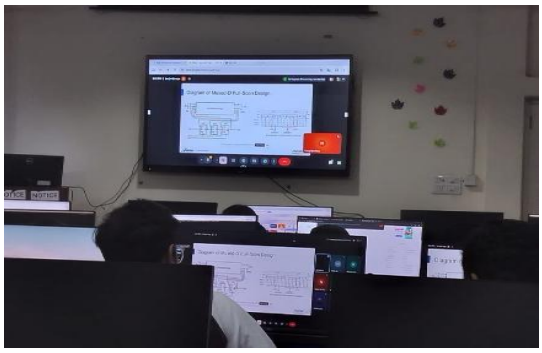
Week 2: Foundation of ASIC Design and RTL Implementation

Date: 13-07-2026 to 17-07-2026

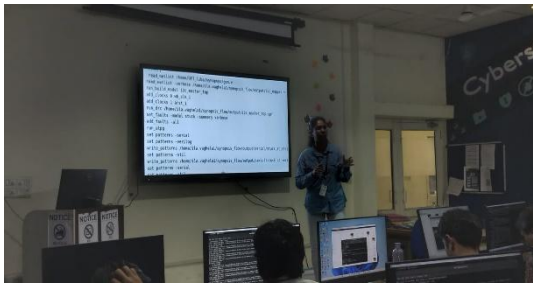
Session Details



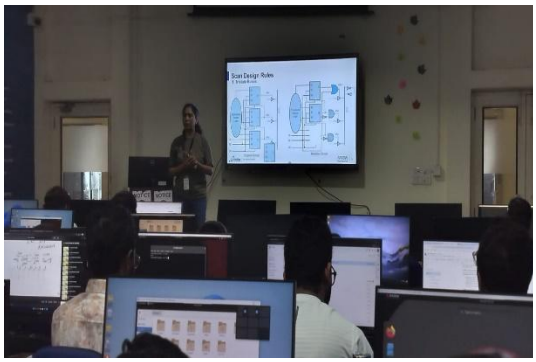
DFT in ASIC Design Flow



Practical session Muxed D Full Scan Design



Assignment Project for Students



Scan Design Rules

Topics covered

Objective:

- To provide participants with an understanding of advanced Design for Testability (DFT) techniques, including scan chain insertion, ATPG, and scan compression methodologies.
- To introduce functional verification concepts and layered testbench architecture used for verifying digital integrated circuits.
- To develop practical skills in System Verilog programming through object-oriented concepts, interfaces, transactions, and verification components.
- To familiarize participants with coverage-driven verification techniques and complete verification flow using industry-standard EDA tools.

Session Details:

- The week commenced with an introduction to the complete ASIC design flow, where participants learned the various stages involved in transforming a digital specification into a fabricated integrated circuit.
- Ms. Ila Vaghela introduced the concepts of ASIC design methodology and explained the significance of each design stage in semiconductor development.
- Ms. Maitri Patel and Mr. Parth Vaghasiya conducted sessions on logic synthesis and semiconductor design methodologies, introducing RTL synthesis, technology mapping, timing analysis, and the semiconductor industry ecosystem.
- Participants gained practical exposure to physical design implementation, including floorplanning, placement, clock tree synthesis, routing, timing verification, and physical sign-off using Synopsys IC Compiler II during the laboratory sessions.
- Mr. Siddhesh Patil introduced Verilog HDL programming concepts and demonstrated structural, dataflow, and behavioural modelling techniques

Felicitation of Industry Expert

Felicitation of Industry Expert


Hands on training session


Hands on Training session

through hands-on implementation of digital circuits.

- The week concluded with sessions on sequential circuit design, finite state machine fundamentals, waveform analysis, and interactive hands-on exercises, followed by daily question-and-answer sessions with the industry experts.

Topics Covered:

- Scan design rules, scan chain insertion, lock-up latches, multi-clock scan chains, and DFT implementation flow.
- ATPG, scan compression, Embedded Deterministic Test (EDT), fault modelling, and test pattern generation.
- Functional verification methodology, layered testbench architecture, verification planning, and mailbox communication.
- System Verilog object-oriented programming, classes, interfaces, transactions, randomization, and verification environment.
- Code coverage, functional coverage, cover groups, cross coverage, and dual-port RAM verification.

Tools Used:

- Synopsys Design Compiler (DFT Compiler)
- Synopsys TetraMAX ATPG
- Synopsys VCS Simulator
- Synopsys Verdi Debugger
- EDA Playground
- SystemVerilog

Learning Outcome:

- Developed practical skills in DFT implementation, SystemVerilog-based functional verification, and coverage-driven verification using industry-standard EDA tools..

Certificate Distribution: