Internship Brief

Title: *RTL to GDSII: From Design to Silicon*
Program: Summer Internship (GTU)
Duration: 16th June 2025 – 25th July 2025
Total Duration: 6 Weeks
Mode: Offline (Hands-on + Theoretical Sessions)

Week 1: Introduction to Verification

The internship began with an orientation and registration session followed by an introductory overview of the internship structure and objectives. The technical journey commenced with a comprehensive introduction to functional verification using Verilog and System Verilog. Interns were guided through the basics of digital design, understanding the role of RTL (Register Transfer Level) design and its significance in the VLSI design flow. The week emphasized simulation strategies and the construction of testbenches, which are crucial for verifying circuit functionality before synthesis.

Week 2: Modeling with Verilog and System Verilog

The second week focused on practical aspects of hardware design using Verilog. Interns gained hands-on experience in modeling both combinational and sequential logic circuits. Special attention was given to understanding the difference between blocking and non-blocking assignments, which is critical in behavioral modeling. The week also introduced System Verilog enhancements, including data types and fundamental object-oriented programming (OOP) principles. These skills helped bridge the gap between simple hardware modeling and advanced verification methodologies.

Week 3: Basics of Design for Testability (DFT)

The third week marked the beginning of the Design for Testability (DFT) module. Interns were introduced to the motivation behind DFT in modern chip design and the challenges associated with post-fabrication testing. Topics covered included scan-based testing, controllability and observability, and common fault models such as stuck-at faults. Sessions on scan chain insertion provided insight into how design structures are modified to enable efficient testing using automatic test equipment (ATE).

Week 4: ATPG and Simulation

This week deepened the understanding of DFT with a focus on Automatic Test Pattern Generation (ATPG). Interns explored techniques for generating effective test vectors to

detect faults with high coverage. Theoretical sessions were followed by simulation practices, helping students validate scan chains and evaluate test quality. Additionally, reverse presentation sessions encouraged interns to revisit and explain previously learned topics, fostering a collaborative and peer-reviewed learning environment.

Week 5: Introduction to Physical Design Flow

Week five transitioned the focus from front-end to back-end VLSI design, specifically Physical Design (PD). The week began with an introduction to the physical design workflow, including concepts like synthesis, floorplanning, and placement. Interns learned how RTL is synthesized into a gate-level netlist and how logic cells are arranged within a chip layout. Detailed sessions on the Place and Route (PnR) process emphasized the optimization of timing, area, and power to meet design constraints.

Week 6: Signoff and Physical Verification

The final week concluded the PD module with in-depth discussions on signoff checks such as Static Timing Analysis (STA), Design Rule Check (DRC), and Layout Versus Schematic (LVS) verification. These processes ensure the physical implementation is correct and ready for fabrication. Interns reviewed the complete RTL-to-GDSII flow and participated in project-based review presentations to consolidate their understanding. The internship culminated with reflections on the holistic journey from digital design conception to physical silicon implementation.