Report

AIU-AADC sponsored FDP on
"Next Gen of Design, Manufacturing, Packaging Semiconductor Technologies"
30 June - 04 July, 2025

Coordinator: Prof. G. D. Makwana
Co-coordinator: Prof. Parth Chauhan

GTU - School of Engineering and Technology organized a five-day Faculty Development Program (FDP) on "Next Generation of Design, Manufacturing, Packaging Semiconductor Technologies" during 30th June – 4th July, 2025.

The objectives of the FDP were:

- To introduce participants to advanced semiconductor process technologies and digital design methodologies
- To build foundational and advanced understanding of ASIC and high-voltage chip design
- To cover emerging topics including AI/ML applications in VLSI, neuromorphic and spintronic devices
- To familiarize participants with modern EDA tools such as Cadence Modus for DFT and ATPG
- To provide exposure to the complete design flow: RTL → synthesis → test → place & route → signoff.

Faculty members and Ph.D. scholars from various institutes across India actively participated in this FDP. In the FDP, there are 85 candidates who are participated from reputed universities/institutes of Gujarat, Maharashtra, Madhya Pradesh, Rajasthan, Bihar, Delhi and from other states. The following experts are invited to deliver session in the FDP.

1. Prof. R. A. Thakker, Director, RDC, GTU
2. Prof. Pradeep Dixit, Associate Professor, IIT Bombay
3. Prof Nihar Mohapatra, Professor, IIT Gandhinagar
4. Prof. Bhagwati Prasad, Asst. Professor, IISc, Bangalure
5. Prof. Anand Darji, Professor, SVNIT, Surat
6. Prof. Vivek Garg, Asst. Professor, SVNIT Surat
7. Prof. Rutu Parekh, Associate Professor, Dhirubhai Ambani University
8. Mr. Parthav Vyas, Director, Scaledge India Pvt. Ltd., Ahmedabad
9. Dr. Nikunj Tahilramani, Sr. Data Scientist,, Data Sentinel Inc
10. Mr. Akash Verma, Sr. Engineer, MicroCircuits Innovations Pvt. Ltd
11. Mr. Nirmit Patel, Fodder, MicroCircuits Innovations Pvt. Ltd
12. Mr. Sanjay G. S. Field Application Engineers, Entuple Technologies Pvt. Ltd., Bengaluru

Date: 30-06-2025

Session-1
FinFET Device Modelling

About Expert: Dr. Rajesh Thakker

Dr. Rajesh Thakker, currently Director of RDC Cell at GTU, holds a Ph.D. and MTech in Microelectronics/VLSI from IIT Bombay. With over 25 years of teaching experience, he specializes in VLSI and image processing, and holds 1 US, 1 European, and 5 Indian patent filings. He has published 50+ research papers, authored a book on evolutionary algorithms in VLSI, and guided 5 completed and 5 ongoing Ph.D. scholars.
Dr. Thakker is also a reviewer for Elsevier and IEEE journals, and has supervised 24 M.E. dissertations

Session Details

FinFET vs GAA Nanosheet

Device – Circuit Fabrication

Topic covered

- FinFET: gate control moderate (wraps 3 sides); GAA: excellent (wraps all sides)
- FinFET scalability limited <3 nm; GAA offers better scalability.
- FinFET has mature manufacturing; GAA is more complex.
- Device fabrication → model development (parameter extraction) → circuit design & simulation.
- Post layout simulation is performed after layout preparation.
- The flow ensures verification at multiple stages before final circuit fabrication.
- Covers full chain from device to final circuit fabrication integrating simulation.

Session-2

Semiconductor Field – A Holistic View

About Expert: Mr. Parthav Vyas

Mr. Parthav Vyas is Site Head at Scaledge India Pvt. Ltd., Ahmedabad, with a rich background in VLSI and semiconductor design. He holds a Master's in Electronics & Communication Systems from DDU (2006) and worked at EInfochips before joining Scaledge in 2013. Having led global teams and worked extensively in the US with top semiconductor firms, he blends deep technical expertise with leadership. Currently pursuing the Senior Management Program at IIM Ahmedabad, he continues to drive innovation in the semiconductor industry.

Session Details

Routing

Tapeout

Topic covered

- Routing connects the placed standard cells using metal interconnect layers to form actual circuit connections.
- It is a crucial step to ensure that signals travel correctly across the chip with minimal delay.
- Routing must carefully avoid congestion, where too many wires crowd a region, which can lead to timing failures.
- It also minimizes signal interference (crosstalk) which can cause logical errors or noise.
- Tape out is the final step where the completely verified chip design is sent to the semiconductor foundry.
- It means generating and delivering the final layout files that describe how the chip will be physically manufactured.
- The slide shows FinFET nodes at 14nm, 10nm, 7nm, and 5nm as examples of advanced technology nodes ready for fabrication.

Session-3
AI/ML in VLSI Design

About Expert: Dr. Nikunj Tahilramani

Dr. Nikunj Tahilramani is a Senior Data Scientist at Data Sentinel Inc., with 13 years of diverse experience across academia, research, and industry. His expertise spans AI, ML, Deep Learning, IoT, Cyber Security, and ECE, supported by 25+ publications in reputed journals. He has held key academic roles, delivered expert sessions at premier institutes like NIT Jaipur and PDEU, and led the ECE department at Silver Oak College. An IEEE Senior Member and ISC2 Candidate (2025), he actively advances innovation in AI and cybersecurity.

Session Details

AI for gate level design

AI/ML in Post Silicon Validation and Yield Prediction

Topic covered

- Discusses ML algorithms at gate-level design like Polynomial Regression for fitting non-linear power/delay models.
- Highlights Radial Basis Function Networks (RBFN) used for delay estimation with good generalization.
- Mentions Bayesian Inference for predicting parameter distributions under noisy conditions, and Regression Splines (RSM) to model delay/power.
- States these ML methods can replace or enhance SPICE-based modeling, speeding up timing closure and early optimization.
- Describes use of regression models to estimate yield from layout density, critical area, and process parameters.
- Helps fabs monitor real-time quality by identifying trends and weak points before they escalate.
- AI/ML reduces costly design re-spins and boosts first-pass silicon success.

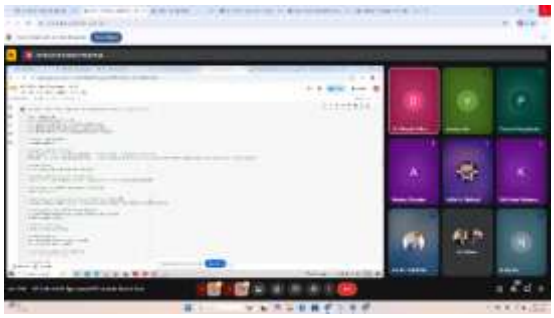
Session-4
Use Cases of AI/ML in VLSI

About Expert: Dr. Nikunj Tahilramani

Session Details

Chip Fault Detection Using AI


Demonstration of implementing code for VLSI fault detection


Random Forest for Timing Delay Prediction

Topic covered

- Discusses challenges in manually detecting faults in VLSI chips due to millions of transistors and complex layouts.
- Highlights how AI techniques, especially image-based methods, help automate fault detection and improve coverage.
- Notes that manual fault detection is expensive and not scalable for dense circuits.
- Demonstrates using CNNs (Convolutional Neural Networks) to classify chip regions as faulty or non-faulty.
- Colab notebook coding example for VLSI chip fault detection using synthetic image data.
- OpenCV to simulate chip layouts and inject synthetic faults (red dots) for training.
- Data that can be fed into a machine learning model for classification.
- Sets up groundwork to automate fault detection using visual features of chip layouts.
- Presents a Python example using Random Forest Regression to predict timing delays in VLSI circuits.
- Simulates data with wire lengths and load capacitance affecting delay, adding measurement noise.

Date: 01-07-2025

Session-5

Next Gen Electronics Substrate

About Expert: Dr. Pradeep Dixit

Dr. Pradeep Dixit is an Associate Professor in Mechanical Engineering at IIT Bombay, with a PhD from NTU Singapore and a master's from IIT Bombay. He previously worked at VTT Finland, developing 3D packaging for MEMS sensors. His expertise spans silicon microfabrication, microsystems packaging, 3D interconnects, and micromachining, with over 75 peer-reviewed publications. He serves as Associate Editor for *Microsystem Technologies* and *Scientific Reports*, and is a Norman Hackerman Young Author Award recipient.

Session Details

IC Packaging Process Flow Diagram

Step-by-Step Semiconductor IC Packaging Stages

Topic covered

- Shows the journey from a silicon wafer (300 mm) to a functional IC chip.
- Highlights single and multi-chip packaging for electrical connections and protection.
- Emphasizes the role of packaging in mechanical support and heat dissipation.
- Illustrates typical packaged ICs used in processors, like Intel Core chips.
- The process starts with a silicon wafer that is sawed into individual dies.
- Each die is attached to a package substrate, then wire bonding connects it electrically.
- Molding, plating, and marking steps protect and label the device.
- Finally, the IC undergoes trimming, singulation, and final testing before shipping.
- This complete packaging process ensures mechanical stability, thermal management, and reliable electrical performance of the final IC.

Session-6

Emerging Trends and Future Prospects in Solar Cell Technology

About Expert: Dr. Vivek Garg

Dr. Vivek Garg is an Assistant Professor in the Department of Electronics Engineering at SVNIT Surat, leading the Optoelectronics2Application research group. His research spans energy harvesting, sensors, quantum technology, and memory devices. He holds a Ph.D. from IIT Indore and has published over 90 papers, including 45 in reputed journals. Dr. Garg is also an IEEE Senior Member and actively reviews for top journals in the field.

Session Details

Wafer Saw and Washer

Semiconductor Packaging

Topic covered

- Shows the process of cutting silicon wafers into individual dies using a dicing blade.
- Highlights the role of DI water to remove silicon dust during sawing.
- Illustrates unsawn and sawn wafers attached to adhesive tape.
- Includes a schematic showing blade action and adhesive tape holding dies.
- Depicts the complete packaging flow from wafer mount to final packing.
- Divides process into FOL (front-end), EOL (back-end), and final test & packing stages.
- Lists critical steps like die attach, wire bonding, molding, plating, and marking.
- Ends with automated testing and packaging into reels or tubes.
- Hence explained all the steps of semiconductor packaging.

Session-7
ASIC design with AI/ML -1

About Expert: Mr. Akash Verma

Akash Verma is an ASIC Physical Design Engineering Lead with extensive experience in advanced deep-sub nanometer technologies. He has spearheaded the design of complex SoCs that power smartphones, data centers, AI accelerators, and modern networking systems. Currently, he leads a venture driving scalable ASIC design frameworks for next-generation semiconductor innovation. Akash stands out as a precision-focused engineer and visionary leader dedicated to pushing the boundaries of technology.

Session Details

SpotON flowcell

Thermal map of floorplan

Topic covered

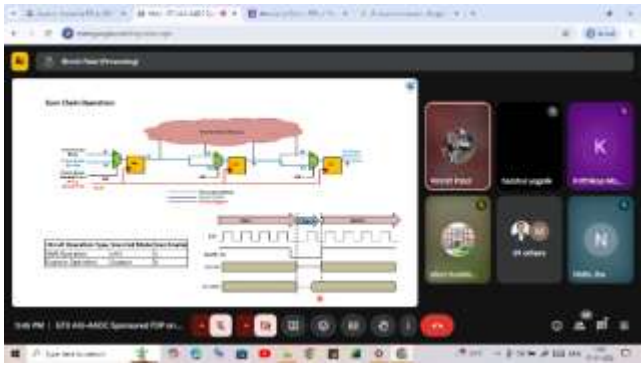
- Shows a thermal analysis of the chip floorplan to identify hotspots.
- Helps optimize power distribution and improve cooling design.
- Visualizes heat density across different functional blocks.
- Critical for ensuring reliability in high-performance ASICs.
- The process starts with a silicon wafer that is sawed into individual dies.
- Each die is attached to a package substrate, then wire bonding connects it electrically.
- Molding, plating, and marking steps protect and label the device.
- Finally, the IC undergoes trimming, singulation, and final testing before shipping.

Session-8
ASIC design with AI/ML -2

About Expert: Nirmit Patel

Nirmit Patel is an ASIC Physical Design Engineering Lead with extensive experience in advanced deep-sub nanometer technologies. He has spearheaded the design of complex SoCs that power smartphones, data centers, AI accelerators, and modern networking systems. Currently, he leads a venture driving scalable ASIC design frameworks for next-generation semiconductor innovation. Mr. Nirmit stands out as a precision-focused engineer and visionary leader dedicated to pushing the boundaries of technology

Session Details



Scan Chain Operation

Significant DFT challenges & AI solutions

Topic covered

- Shows how scan chains connect flip-flops to test combinational logic.
- Illustrates functional vs. scan paths with separate data and control signals.
- Highlights shift-in, capture, and shift-out operations in test cycles.
- Table summarizes scan cell modes for shifting (SE=1) and capturing (SE=0).
- AI helps optimize scan compression ratios, reducing guesswork and improving test efficiency.
- It selects the best high-level DFT architecture by analyzing SoC topology and project needs.
- Automates debugging to close the final 1% of test coverage, identifying root causes.
- Speeds up silicon failure analysis by linking test failures to layout and fabrication data..

Date: 02-07-2025

Session-9

Semiconductor Fabrication Technologies

About Expert: Dr. Vivek Garg

Session Details

Semiconductor Applications

Semiconductor Device Applications

Topic covered

- Highlighted diverse semiconductor applications in power electronics, RF & wireless communication, memory, and photonics.
- Emphasized MEMS, sensing, imaging, and their roles in smart systems.
- Discussed advanced packaging like TSV, 2.5D/3D IC integration for enhanced performance.
- Covered emerging materials, substrates, and next-gen compound semiconductors.
- Illustrated the wide usage of semiconductor devices in communication products like phones, tablets, and PCs.
- Highlighted applications in home electronics, including TVs, game consoles, and kitchen appliances.
- Showed their role in infrastructure and industrial automation, from surveillance systems to robots.
- Emphasized the central place of semiconductor chips powering diverse modern technologies.

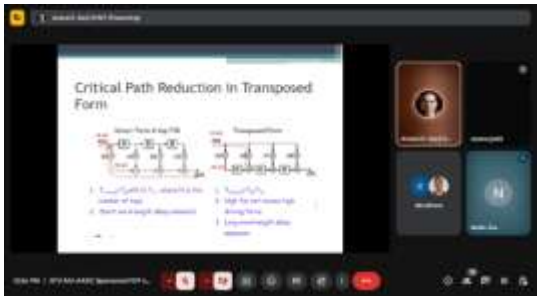
Session-10

DSP VLSI architecture optimization Techniques

About Expert: Dr. Anand Darji

Dr. Anand Darji is a Professor in the Department of Electronics Engineering at SVNIT Surat with over 23 years of teaching and research experience. He earned his B.Tech from B.V.M. and M.Tech & Ph.D. in Microelectronics from IIT Bombay. His work spans MEMS sensors, VLSI & FPGA design, embedded systems, and biomedical signal processing, with 80+ publications.
Dr. Darji has led multiple funded projects, successfully taped out 3 chips, and served as program chair for VDAT-2021.

Session Details



Critical Path Reduction in Transposed Form

Iteration Bound – Fundamental Limit

Topic covered

- Compared direct form 4-tap FIR filter with transposed form to analyze timing.
- Direct form shows critical path depends on the number of taps, increasing delay.
- Transposed form reduces critical path but introduces high fan-out issues.
- Highlights trade-off: shorter critical path vs long word-length delay elements.

- Shows three structural forms of carbon nanotubes: armchair, zigzag, and chiral.
- Highlights how arrangement impacts electrical and mechanical properties.
- Symmetry defines whether a CNT behaves metallic or semiconducting.
- This classification is key for nanodevice and sensor applications.

Session-11
Advance ASIC Design Flow -1

About Expert: Mr. Sanjay G S

Mr. Sanjay G S is a skilled professional in VLSI design, currently working as a Field Application Engineer at Entuple Technologies Pvt. Ltd. He completed his B.Tech from BNM Institute of Technology, Bengaluru in 2024 and has experience with ASIC, FPGA, and SoC architectures. Alongside his technical work, he serves as Deputy Software Lead at LAMP, a nonprofit, since 2022. Sanjay holds a Cadence-certified badge in RTL-to-GDSII, reflecting his strong capabilities in silicon design and implementation flows.

Session Details

What matters in VLSI?

CIC Flow

Topic covered

- Traced Intel processor evolution from 45nm to 7nm nodes.
- Showed increased cores, speed, and memory with each generation.
- Linked smaller nodes to better power, area, and performance.
- Underlined key VLSI design focus on power, performance, area (PPA).
- Illustrated the custom IC flow using Cadence Virtuoso tools.
- Covered schematic entry, simulation, layout, and verification.
- Included DRC/LVS checks and RC extraction before tape-out.
- Final GDSII file prepares design for semiconductor fabrication.
- Emphasized iterative optimization at each stage to meet stringent design specifications.
- Highlighted how advanced EDA tools streamline complex analog and mixed-signal design processes.

Session-12
Advance ASIC Design Flow -II

About Expert: Mr. Sanjay G S

Session Details

Introduction to DFT


Timing Debug-Cadence

Topic covered

- Explained DFT (Design for Testability) to improve circuit test coverage.
- Mentioned insertion of DFT during early design flow like RTL synthesis.
- Enhanced controllability and observability of internal circuit nodes.
- Presented a typical VLSI ASIC design flow highlighting DFT integration.
- Demonstrated timing analysis using Cadence tools for ASIC design flow.
- Showed a path histogram indicating distribution of critical paths and slack.
- Listed categories and detailed path list with delay, slack, and endpoints.
- Highlighted the graphical circuit layout alongside timing debug results.
- Facilitated efficient timing closure by visually correlating critical paths with physical layout, enabling targeted optimizations.

Date: 04-07-2025

Session-13

Next Gen Devices – CMOS

About Expert: Dr. Nihar Ranjan Mohapatra

Dr. Nihar Ranjan Mohapatra is a Professor at IIT Gandhinagar, where he leads the NanoDC Lab with pioneering research in computational nanoelectronics, nanoscale device physics, process integration, and IC design. A Ph.D. from IIT Bombay and an INTEL Research Fellow, he has rich industry experience from his roles at AMD, GLOBALFOUNDRIES in Germany, and IHP Microelectronics. A University Gold Medalist, Dr. Mohapatra's impactful work in device modeling, semiconductor reliability, and CMOS technology has earned wide recognition. Since joining IITGN in 2011, he has been instrumental in advancing nanoelectronics research and mentoring the next generation of innovators.

Session Details

Transport of Electrons – Drain Current

FinFET based CMOS Technology

Topic covered

- This slide explains the electron transport mechanism in MOSFETs
- It presents the mathematical expressions for drain current (ID) in both linear and saturation regions based on gate and drain voltages.
- The visuals illustrate the movement and accumulation of carriers.
- It highlights how channel formation and current conduction depend on gate-source voltage (Vgs) surpassing the threshold voltage (Vth).
- Illustrates a FinFET structure showing source, drain, gate, and well tie, emphasizing the fully depleted body.
- Discusses advantages such as increased Ion and gm per area, less DIBL, negligible body effect, and better control due to quantized channel width.

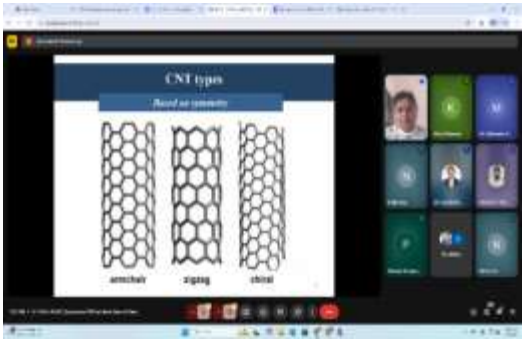
Session-14
Nano electronics

Expert: Dr. Rutu Parekh

Dr. Rutu Parekh is an Associate Professor at DA-IICT, Gandhinagar, specializing in micro/nanoelectronics, nanofabrication, and analog mixed-signal design. She holds an M.Eng. from Concordia University and a Ph.D. in Nanoelectronics from Université de Sherbrooke, with postdoctoral work at IIT Bombay. Her diverse experience spans research at École Polytechnique de Montréal, industry roles at eInfochips and HP, and teaching at Nirma University. An active researcher and editorial board member, she has numerous international publications and contributions to technical committees worldwide..

Session Details

The Scale of Things – Nanometers and More



CNT Types Based on Symmetry

Topic covered

- Compares natural and manmade objects across a scale from meters to nanometers.
- Shows how DNA, ATP synthase, and atoms lie deep in the nanoworld.
- Illustrates microdevices like MEMS and quantum structures at the nano level.
- Highlights the challenge of manipulating matter precisely at atomic scales.
- Shows three structural forms of carbon nanotubes: armchair, zigzag, and chiral.
- Highlights how arrangement impacts electrical and mechanical properties.
- Symmetry defines whether a CNT behaves metallic or semiconducting.
- This classification is key for nanodevice and sensor applications.
- The chirality (armchair, zigzag, or chiral) determines electronic properties of CNTs.

Session-15
Advance ASIC Design Flow -III

About Expert: Mr. Sanjay G S

Session Details

Introduction to DFT

Terminal with Genus Synthesis

Topic covered

- Explained DFT (Design for Testability) as adding test features into IC design.
- Discussed controllability and observability for improved circuit testing.
- Presented VLSI ASIC design flow with stages from RTL to GDSII.
- Emphasized how DFT fits into the overall chip design and verification process.
- Demonstrated loading of libraries and executing scripts for Genus Synthesis in a Linux environment.
- Showed process of reading 90nm standard cell libraries essential for synthesis.
- Highlighted terminal commands and tool initialization for synthesis flow.
- Provided practical exposure to working with synthesis tool commands and library checks.

Session-16
Advance ASIC Design Flow -II

About Expert: Mr. Sanjay G S

Session Details

DFT Techniques


script.tcl for synthesis

Topic covered

- Highlights key Design for Test (DFT) techniques used in VLSI industry.
- Lists Automatic Test Equipment (ATE) and Automatic Test Pattern Generation (ATPG) for testing.
- Mentions Built-in Self Test (BIST) and Boundary Scan methods to improve test coverage.
- Includes a diagram showing scan flip-flops inserted in logic for easy fault detection.
- Demonstrates a TCL script automating digital synthesis for a counter design.
- Reads libraries, design HDL files, and input constraints for synthesis setup.
- Generates timing, area, and power reports, and writes out netlist and constraints.
- Final commands export synthesized gate-level Verilog and launch the GUI for review.

Date: 04-07-2025

Session-17
Materials-Devices & Packaging

About Expert: Dr. Bhagwati Prasad

Dr. Bhagwati Prasad is an Assistant Professor at IISc Bangalore, specializing in materials engineering. He earned his Ph.D. in Materials Science from the University of Cambridge and has collaborated with premier institutes like UC Berkeley, Max Planck, and Western Digital. His pioneering research in spintronics, neuromorphic computing, and AI hardware has led to 30+ papers and 30+ patents. With a journey from IIT Kanpur to Cambridge to IISc, he brings exceptional global expertise shaping future electronics and memory technologies.

Session Details

Scaling of Semiconductor Memory Devices

Memory and Storage Technologies

Topic covered

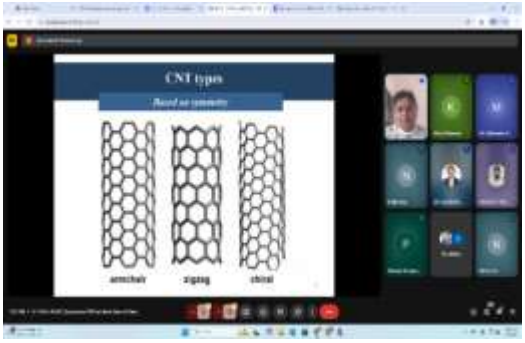
- Shows 3D NAND integration with 300+ layers by Kioxia & Western Digital.
- Illustrates how vertical stacking improves density and storage.
- Enables more data on smaller footprints, boosting performance.
- Important for next-gen memory and cost-efficient large-scale storage..
- Compares volatile memory (DRAM, SRAM) vs. nonvolatile (Flash, MRAM).
- Highlights emerging tech like STT RAM, R RAM, CNT memory, FeRAM.
- Storage side includes HDD, NAND Flash, Optical, Magnetic Tape.
- Shows industry branching into multiple specialized memory/storage paths.
- Hence explained all kinds of memory and their application.

Session-18
High Voltage Chip Design

About Expert: Dr. Rutu Parekh

Session Details

The Scale of Things – Nanometers and More



CNT Types Based on Symmetry

Topic covered

- Compares natural and manmade objects across a scale from meters to nanometers.
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- Highlights how arrangement impacts electrical and mechanical properties.
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Session-19
Advance ASIC Design Flow -V

About Expert: Mr. Sanjay G S

Session Details

Synthesis Flow with DFT

Physical Design Flow

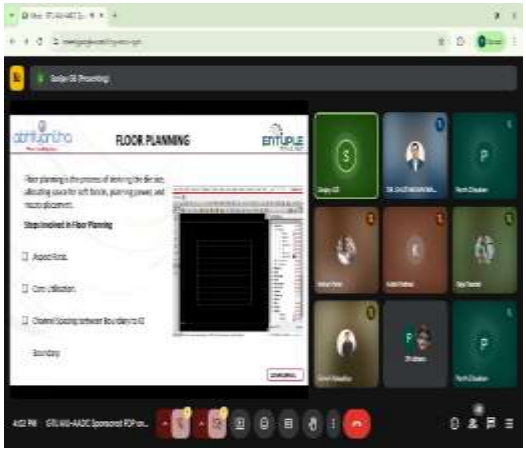
Topic covered

- Illustrated synthesis starting from technology files, RTL, and constraints.
- Steps covered loading design, setting constraints and scan style for testability.
- Highlighted generic synthesis followed by gate-level optimization.
- Concluded with writing final outputs for downstream implementation.).
- Presented the complete flow from gate-level netlist to GDS-II layout.
- Included stages: floor planning, power planning, placement, and clock tree synthesis.
- Followed by routing, RC extraction, and final physical verification.
- Ensured design readiness for tape-out through systematic, tool-driven flow.

Session-20
Advance ASIC Design Flow -VI

About Expert: Mr. Sanjay G S

Session Details



Floorplanning

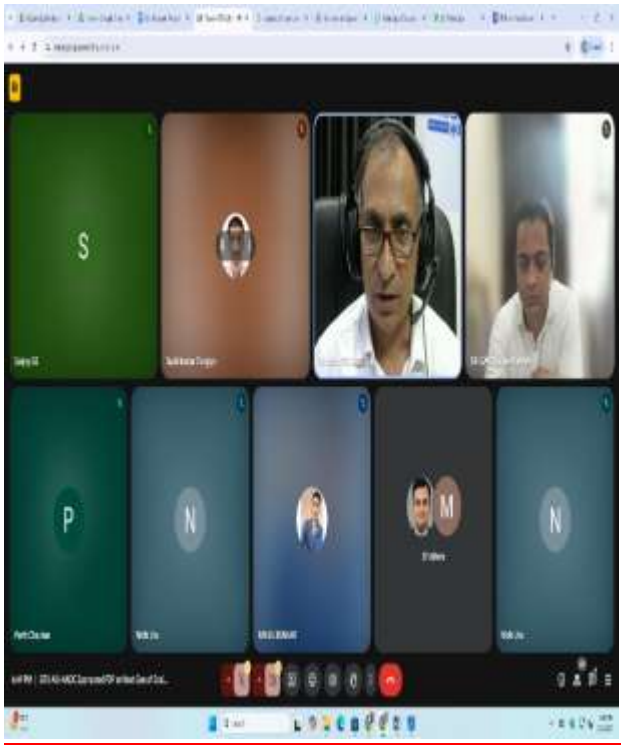
Synthesis Script in Genus-Cadence and Result

Topic covered

- Explained floor planning to determine die size and macro placement.
- Addressed key steps: managing aspect ratio, optimizing core utilization.
- Discussed spacing channels between boundaries and IOs for efficient routing.
- Visualized layout tool snapshot showcasing block and boundary placement.
- Demonstrated TCL script automating synthesis steps like reading libraries, elaborating design, and applying constraints.
- Generated reports on timing, area, and power along with final netlist and constraints file.
- Verified scan chains, reporting detection of multiple scan chains and default patterns.
- Successfully built FULLSCAN mode, confirming the synthesis and test structures.

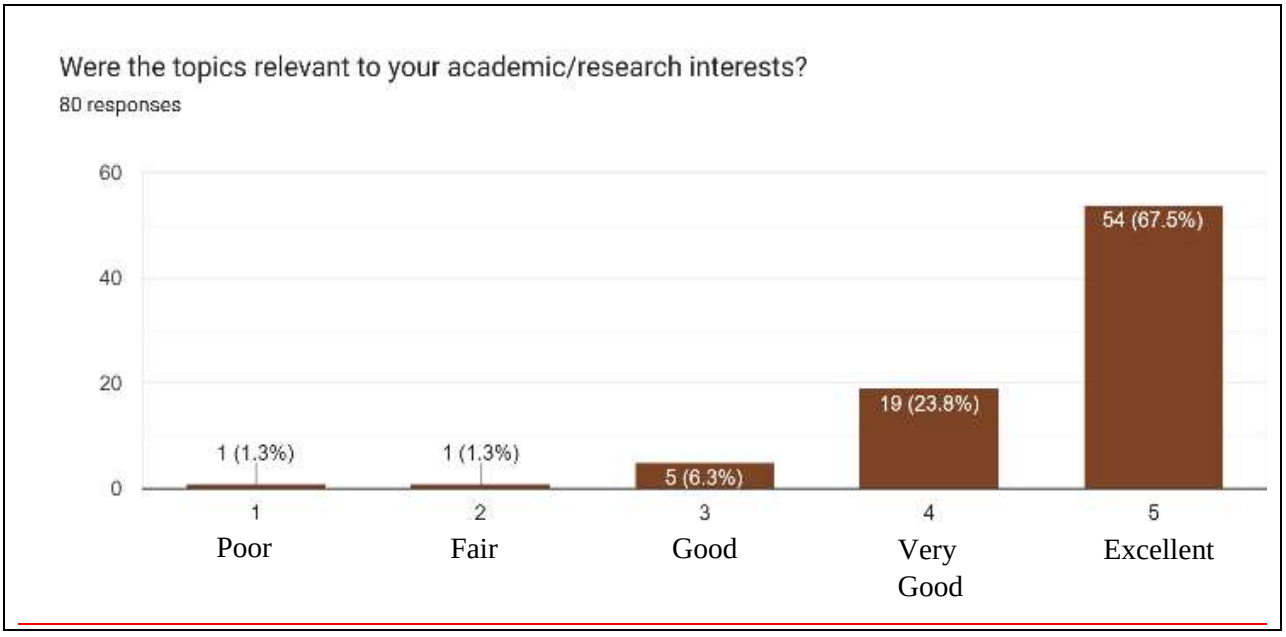
Date: 04-07-2025

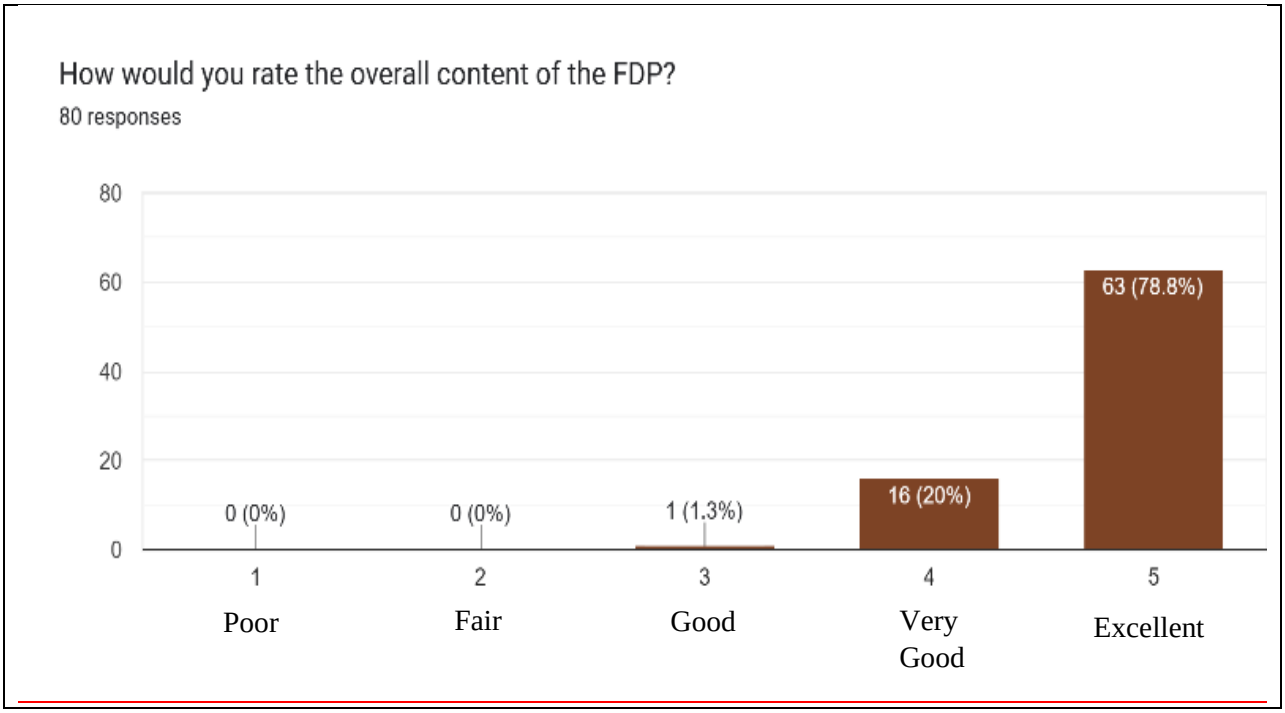
CONCLUDING REMARKS



The session concluded with an expression of gratitude by Prof. Parth Chauhan, Co-coordinator of the FDP, who delivered the formal vote of thanks. Dr. Gautam Makwana, Coordinator, also extended his appreciation to the esteemed experts and all participants for their active engagement. Dr. R.A. Thakkar, Director of RDC Cell, GTU, conveyed his sincere gratitude, underscoring the significance of such programs in advancing the university's academic and research vision. Additionally, feedback forms were collected, and a comprehensive assessment comprising 100 MCQs was administered to participants to evaluate their understanding and reinforce key concepts. Several participants also expressed their enthusiasm for deeper technical exposure, proposing that future sessions include a full-day hands-on workshop on specific industry-standard tools, thereby charting the course for the next phase of skill enhancement.

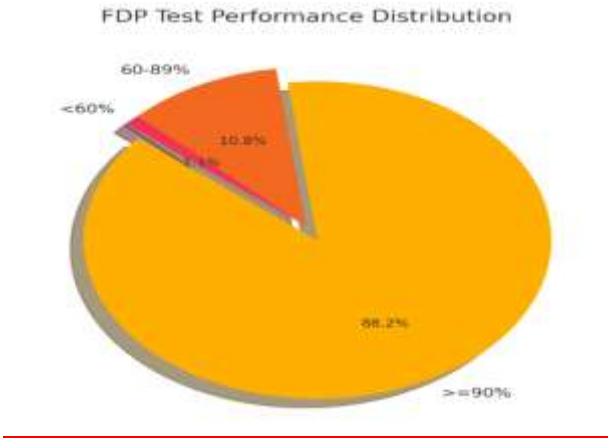
FEEDBACK OF PARTICIPANTS:





The FDP received an overwhelming positive response, with over 95% of participants rating the session content as either 4 or 5**,** indicating high satisfaction. Specifically, 67.5% of attendees rated the session content at the highest level (5), reflecting the perceived excellence of the technical material delivered. Regarding the overall content of the FDP, nearly 79% awarded it the top rating (5)**,** underscoring the program's success in aligning with participant expectations. These strong feedback scores highlight the program's effective design and delivery, and also point toward enthusiastic interest for deeper sessions on specific tools in future editions.

ASSESMENT OF PARTICIPANTS:



1. A total of **participants** took the test consisting of **100 MCQs** designed to assess understanding of **topics covered in the FDP**.
2. The **average score is an impressive ~95.5%**, with the highest score being a perfect **100%**, and the lowest at **36%**.
3. Notably, **82 participants scored 90% or above**, indicating excellent grasp of the content delivered, while only **1 participant scored below 60%**.

GUJARAT TECHNOLOGICAL UNIVERSITY

SCHOOL OF ENGINEERING AND TECHNOLOGY

AIU-AADC sponsored Online FDP on "Next Gen of Design, Manufacturing, Packaging Semiconductor Technologies"

30/06/2025 to **04/07/2025**

List of Participants				
Sr. No.	**Name**	**Designation**	**Institute**	**Reference No**
1	DR AMRUTBHAI PATEL	Associate Professor	GUNI UVPCE	GTU/SET/2025/07/08/FDP/CERTI/01
2	NUPUR GIRISH NANOTI	Research Scholar	Symbiosis International (Deemed) University, Pune	GTU/SET/2025/07/08/FDP/CERTI/02
3	URJITSINH I RATHOD	Ph.D. Scholar	Saurashtra University	GTU/SET/2025/07/08/FDP/CERTI/03
4	KINJAL BHAVSAR	Lecturer	VPMP Polytechnic	GTU/SET/2025/07/08/FDP/CERTI/04
5	MOHIT KUMAR DUBEY	Assistant professor	GOVT MJS PG College Bhind MP	GTU/SET/2025/07/08/FDP/CERTI/05
6	JAGDISH RATHOD	Head of Department (Electrical Engineering)	Tolani Foundation Gandhidham Polytechnic	GTU/SET/2025/07/08/FDP/CERTI/06
7	PRIYANKA SINGHVI	Assistant professor	College of Technology and Engineering ,Udaipur	GTU/SET/2025/07/08/FDP/CERTI/07
8	KETANKUMAR JAYANTILAL PATEL	Assistant Professor	U. V. PATEL COLLEGE OF ENGINEERING	GTU/SET/2025/07/08/FDP/CERTI/08
9	BUNKAR RAHUL SINGH MUNNALAL	Student	GOVERNMENT POLYTECHNIC NAVSARI 975	GTU/SET/2025/07/08/FDP/CERTI/09
10	LAVANYA B L	Assistant Professor	NMAMIT Nitte	GTU/SET/2025/07/08/FDP/CERTI/10
11	DR. SATHEESH RAO	Assistant Professor Gd III	NMAM Institute of Technology, Nitte	GTU/SET/2025/07/08/FDP/CERTI/11
12	DR ROBINSON PAUL	Assistant Professor	BVM	GTU/SET/2025/07/08/FDP/CERTI/12
13	DR. VIPULKUMAR M DABHI	Associate Professor	Indrashil University, Kadi	GTU/SET/2025/07/08/FDP/CERTI/13
14	KARAVADRA DEVANSHI ASHOKBHAI	Ph.D. Scholar	GTU	GTU/SET/2025/07/08/FDP/CERTI/14
15	DR. KETKI C. PATHAK	Associate Professor	Sarvajanik College of Engineering and Technology	GTU/SET/2025/07/08/FDP/CERTI/15
16	KRITHIKAA MOHANARANGAM	Assistant Professor	Symbiosis Institute of Technology, Pune	GTU/SET/2025/07/08/FDP/CERTI/16
17	MARSHIANA.D	associate Profesor	Symbiosis Institute of Technology	GTU/SET/2025/07/08/FDP/CERTI/17

18	DINESH KUMAR SAIN	Assistant professor	University college of engineering and technology, Bikaner Technical University, Bikaner	GTU/SET/2025/07/08/FDP/CERTI/18
19	VAIBHAV KUMAR GUPTA	Assistant Professor	The LNM Institute of Information Technology (LNMIIT), Jaipur	GTU/SET/2025/07/08/FDP/CERTI/19
20	PARMAR ROHITKUMAR RANCHHODBHAI	Assistant Professor	G H Patel College of Engineering and Technology, Vallabh Vidyanagar	GTU/SET/2025/07/08/FDP/CERTI/20
21	DR. SHILPA HUDNURKAR	Assistant Professor	Symbiosis Institute of Technology, Pune	GTU/SET/2025/07/08/FDP/CERTI/21
22	PARTHESH MANKODI	Assistant Professor	G H Patel College of Engineering & Technology	GTU/SET/2025/07/08/FDP/CERTI/22
23	JIGNESH JOSHI	Assistant Professor	V V P Engineering College	GTU/SET/2025/07/08/FDP/CERTI/23
24	DR PRIYANKA TUPE WAGHMARE	Assistant Professor	Symbiosis Institute of Technology Pune	GTU/SET/2025/07/08/FDP/CERTI/24
25	ASIF SAYEED KHAN	Assistant Professor	Mahila Engineering College, Ajmer	GTU/SET/2025/07/08/FDP/CERTI/25
26	DR. MOUSUMI BHANJA	Assistant Professor	Symbiosis Institute of Technology Pune	GTU/SET/2025/07/08/FDP/CERTI/26
27	PATEL VINABEN SHANKARBHAI	ASSISTANT PROFESSOR	VIDUSH SOMANY INSTITUTE OF TECHNOLOGY & RESEARCH, KADI	GTU/SET/2025/07/08/FDP/CERTI/27
28	NEELIMA R KOHARE	Associate Professor	COEPTECH	GTU/SET/2025/07/08/FDP/CERTI/28
29	SANJAYKUMAR K PARCHANDEKAR	Associate Professor	Walchand College of Engineering, Sangli	GTU/SET/2025/07/08/FDP/CERTI/29
30	DR. CHANDAN KUMAR CHOUBEY	Assistant Professor	Symbiosis Institute of Technology, Pune	GTU/SET/2025/07/08/FDP/CERTI/30
31	HARSHITA KUSHWAH	Assistant Professor	SHRI GOVINDRAM SEKSAERIA INSTITUTE OF TECHNOLOGY AND SCIENCE (SGISTS)	GTU/SET/2025/07/08/FDP/CERTI/31
32	DR PALLAV RAWAL	Associate Professor	Swami Keshvanand Institute of Technology, Management and Gramothan, Jaipur	GTU/SET/2025/07/08/FDP/CERTI/32
33	PAYAL SHAH	Assistant Professor	LDRP-ITR	GTU/SET/2025/07/08/FDP/CERTI/33
34	GLORIA JOSEPH	Assistant professor	SWAMI KESHVANAND INSTITUTE OF TECHNOLOGY	GTU/SET/2025/07/08/FDP/CERTI/34
35	ASHISH B. RAVALIA	Assistant professor	Department of Nanoscience and Advanced Materials, Saurashtra University, Rajkot	GTU/SET/2025/07/08/FDP/CERTI/35
36	DR. PRATIBHA SHINGARE	ASSISTANT PROFESSOR	COEP TECHNOLOGICAL UNIVERSITY PUNE	GTU/SET/2025/07/08/FDP/CERTI/36

37	VANIA PURVIKKUMAR C	Assistant Professor	LDRP -ITR	GTU/SET/2025/07/08/FDP/CERTI/37
38	DR. AKSHAY GAJANAN BHOSALE	Assistant Professor	Symbiosis Institute of Technology, Pune	GTU/SET/2025/07/08/FDP/CERTI/38
39	SANDEEP SINGH VASIR	PhD Scholar	Gujarat Technological University	GTU/SET/2025/07/08/FDP/CERTI/39
40	HARSHUL YAGNESHBHAI YAGNIK	Assistant Professor	Gujarat Technological University	GTU/SET/2025/07/08/FDP/CERTI/40
41	DR. HARISH CHANDRA KUMAWAT	Assistant Professor	The LNM Institute of Information Technology, Jaipur	GTU/SET/2025/07/08/FDP/CERTI/41
42	PRUTHABA JADEJA	Research scholar	RK University	GTU/SET/2025/07/08/FDP/CERTI/42
43	MAHITCHA UTPAL RASIKLAL	Lecturer in Electrical engineering	Tolani f g polytechnic, Adipur	GTU/SET/2025/07/08/FDP/CERTI/43
44	DR. AMIT CHOKSI	Assistant Professor	Birla Vishvakarma Mahavidyalaya Engineering College	GTU/SET/2025/07/08/FDP/CERTI/44
45	PRANAV B LAPSIWALA	Associate Professor	Sarvajanik College of Engineering & Technology	GTU/SET/2025/07/08/FDP/CERTI/45
46	SUSHMA PARIHAR	Assistant Professor	Symbiosis Institute of Technology, Pune	GTU/SET/2025/07/08/FDP/CERTI/46
47	SUSHILKUMAR PRAKASHBHAI DANGIYA	Visvesvaraya PhD Scholar	GTU - School of Engineering and Technology	GTU/SET/2025/07/08/FDP/CERTI/47
48	VISHAL H SHAH	Assistant Professor	Birla Institute of Technology Mesra	GTU/SET/2025/07/08/FDP/CERTI/48
49	MS SEJAL P VYAS	Ph.D Scholar GTU SET	GTU-SET	GTU/SET/2025/07/08/FDP/CERTI/49
50	SUHANI JATIN CHAUHAN	Assistant Professor	C. K .Pithawala College of Engineering & Technology	GTU/SET/2025/07/08/FDP/CERTI/50
51	HETAL V. DAVE	Ph.D. scholar	GTU	GTU/SET/2025/07/08/FDP/CERTI/51
52	VAISHALIBEN BABULAL PATEL	Asst. Professor	U. V. Patel College of Engineering	GTU/SET/2025/07/08/FDP/CERTI/52
53	DR CHARUSHILA AXAY PATEL	Sr Lecturer	B V Patel Institute of Technology (DS)	GTU/SET/2025/07/08/FDP/CERTI/53
54	TANMAY H BHATT	ASSISTANT PROFESSOR	College of FPTBE , AAU Anand	GTU/SET/2025/07/08/FDP/CERTI/54
55	DR. YOGITA DINKAR KAPSE	Assistant Professor	COEP Tech Univ Pune	GTU/SET/2025/07/08/FDP/CERTI/55
56	BHIMANI NENSI DHANSUKHBHAI	Research Scholar	RK University	GTU/SET/2025/07/08/FDP/CERTI/56
57	SOLANKI MONICA GATURBHAI	Assistant Professor	OM ENGINEERING COLLEGE, JUNAGADH	GTU/SET/2025/07/08/FDP/CERTI/57
58	ABHISHEK PANCHAL	Assistant Professor	UIT RGPV BHOPAL	GTU/SET/2025/07/08/FDP/CERTI/58
59	KASHYAP MUKESHBHAI GANDHI	lecturer	Tolani F G Polytechnic Adipur	GTU/SET/2025/07/08/FDP/CERTI/59
60	TEJAL TANDEL	Assistant Professor	MBIT	GTU/SET/2025/07/08/FDP/CERTI/60

61	ASIFIQBAL Y THAKOR	Assistant Professor	CHARUSAT UNIVERSITY	GTU/SET/2025/07/08/FDP/CERTI/61
62	RITESHKUMAR BHIKHUBHAI VAGHASIYA	ASSISTANT PROFESSOR	DR.SUBHASH UNIVERSITY	GTU/SET/2025/07/08/FDP/CERTI/62
63	ABHISHEK SHARMA	Associate Professor	LNMIIT	GTU/SET/2025/07/08/FDP/CERTI/63
64	MANOJ KUMAR	Assistant Professor	MITS GWALIOR	GTU/SET/2025/07/08/FDP/CERTI/64
65	DR. VIDYA NITIN MORE	Assistant Professor	COEP Technological University Pune	GTU/SET/2025/07/08/FDP/CERTI/65
66	RISHI SAXENA	Assistant Professor	SVIT Vasad	GTU/SET/2025/07/08/FDP/CERTI/66
67	DR. DURGA PRASAD MISHRA	Assistant Professor	The LNMIIT. Jaipur, Rajasthan, India	GTU/SET/2025/07/08/FDP/CERTI/67
68	ABHINANDAN JAIN	Assistant Professor	SKI M & G JAIPUR	GTU/SET/2025/07/08/FDP/CERTI/68
69	SUMANA HAJRA	Ph.D scholar	Department of Nanoscience and Advanced Materials, Saurashtra University	GTU/SET/2025/07/08/FDP/CERTI/69
70	UJJWAL SINGH	Ph.D. Scholar	IIT Jodhpur	GTU/SET/2025/07/08/FDP/CERTI/70
71	DR. HITESH SHAH	Professor	GCEt	GTU/SET/2025/07/08/FDP/CERTI/71
72	DR. DEEPLAXMI V. NITURE	Assistant Professor	COEP Technological University	GTU/SET/2025/07/08/FDP/CERTI/72
73	PRAJAPATI NIMESHKUMAR DAMODARBHAI	Lecturer in Electrical Engineering	Tolani Foundation Gandhidham Polytechnic Adipur Kutch	GTU/SET/2025/07/08/FDP/CERTI/73
74	PRAJAPATI SWAPNILMANUBHAI	PS to Director (Admin) - GUVNL	Gujrata Technological University	GTU/SET/2025/07/08/FDP/CERTI/74
75	DR R RAJALAKSHMI	Associate Professor	Panimalar engineering College, Chennai.	GTU/SET/2025/07/08/FDP/CERTI/75
76	GANATRA KHUSHAL SURESHBHAI	Lab Assistant	Atmiya University	GTU/SET/2025/07/08/FDP/CERTI/76
77	NIDHI JHA	Ph.D. Scholar	GTU-School of Engineering and Technology	GTU/SET/2025/07/08/FDP/CERTI/77
78	SAMIKSHA SINGH CHAUHAN	Assistant Professor	Rewa Engineering College Rewa Madhya Pradesh	GTU/SET/2025/07/08/FDP/CERTI/78
79	UJWALA KSHIRSAGAR	Associate Professor	Symbiosis Institute of Technology, Pune	GTU/SET/2025/07/08/FDP/CERTI/79
80	NIRAV PRAVINCHANDRA MANIAR	Professor	V. V. P. Engineering College	GTU/SET/2025/07/08/FDP/CERTI/80
81	PARTH CHAUHAN	Assistant Professor	GTU-School of Engineering and Technology	GTU/SET/2025/07/08/FDP/CERTI/81
82	RITISHA BHATT	Assistant Professor	GTU-School of Engineering and Technology	GTU/SET/2025/07/08/FDP/CERTI/82

83	PROF. GAUTAM D. MAKWANA	Associate Professor	GTU-School of Engineering and Technology	GTU/SET/2025/07/08/FDP/CERTI/83
84	PROF. S. K. HADIA	Associate Professor	GTU-School of Engineering and Technology	GTU/SET/2025/07/08/FDP/CERTI/84
85	MR. BHARAT DARJI	Lab. Tech.	GTU-School of Engineering and Technology	GTU/SET/2025/07/08/FDP/CERTI/85