GTU Briefing

Gujarat Technological University (GTU) is a State University, NAAC A+ Accredited and premier academic and research institution which has driven new ways of thinking since its establishment in 2007. Today, GTU is an intellectual destination that draws inspired scholars to its campus, keeping GTU at the nexus of ideas that challenge and change the world. More than 350 institutes of Gujarat are affiliated with the GTU. The University caters to the fields of Engineering, Architecture, Management, Pharmacy and Computer Science. GTU has research and skill-based ecosystem in various emerging fields for the benefits of the stakeholders of the University.

GTU-SET

GTU School of Engineering and Technology (GTU-SET) established in 2017 by the GTU. It offers 2- years PG programs in Computer Engineering (Cyber Security), Internet of Things, Artificial Intelligence & Data Science, Civil Engineering (Structure Engineering), VLSI Design and 4 years UG programs in Computer Engineering and Electronics Communication Engineering. All programs are approved by the AICTE, New Delhi. The school offers full-time Ph.D. Programs in Computer Engineering, Electronics & Communication Engineering and Civil Engineering. The school is known to generate manpower with the state-of-the-art technical knowledge in the respective specialized fields. The school has Coe's in Block chain and BOSCH Automation, AICTE Idea and ISEA sponsored laboratories and other state-of-the-art research laboratories.

AIU-AADC Sponsored Faculty Development Program

On

"Next Gen of Design, Manufacturing, Packaging Semiconductor Technologies"

30th June to 4th July, 2025

Organized by

Gujarat Technological University

School of Engineering and Technology,

Academic Block-5, GTU Campus, Chandkheda, Ahmedabad, 382424

Online Link

AIU - FDP on Recent Trends of Design, Manufacturing, Packaging Semiconductor Technologies

30th June, 2025 to 4th July, 2025

Time zone: Asia/Kolkata

Google Meet joining info

Video call link:

https://meet.google.com/khg-smpc-qjm

Or dial: (US) +1 413-752-4053 PIN: 999 549 514#

FDP Details

Objectives of the FDP are:

- To explore recent design methodologies, manufacturing and packaging techniques for development of workforce in the semiconductor technologies
- To nurture various research & development opportunities for the development of the ecosystem
- To connect research organizations, industries and institutions for next-generation strategic and industry-needed design and development

Chief Patron

Dr. Rajul K. Gajjar, Hon'ble Vice Chancellor, GTU

Patron

Dr. K. N. Kher, Registrar, GTU

Convenor

Prof. J. A. Amin, Professor, GTU-SET

Prof. Rajesh A. Thakker, Director, RDC, GTU

Coordinator

Prof. Gautam D. Makwana, Associate Professor, GTU-SET

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Co-Coordinator

Prof. Parth Chauhan, Assistant Professor, GTU-SET

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Session Details

Day-1

The session began with an overview of next-generation power devices, highlighting advanced materials like GaN and SiC for efficient, high-performance power electronics. This was followed by a comprehensive view of the semiconductor industry, covering the entire value chain from raw materials to chip packaging and global market trends. After the lunch break, the focus shifted to semiconductor manufacturing instruments, including tools used in photolithography, deposition, and testing. The final session explored co-packaged optics, emphasizing high-speed, and low-power data transmission solutions.

Day-2

The session started with a discussion on next-generation electronics substrates, focusing on advanced packaging technologies, high-density interconnects, and materials enabling improved electrical performance and thermal management. This was followed by an overview of the physical design flow for advanced technology nodes, covering stages like floor planning, placement, clock tree synthesis, routing, and signoff in sub-10nm processes. After the lunch break, the sessions focused on design for testability (DFT) in semiconductor ICs, emphasizing scan insertion, boundary scan, and built-in self-test techniques to enhance fault detection and ensure manufacturability.

Day-3

The session began with an introduction to predictive modelling and co-design, emphasizing simulation-driven approaches for system-level optimization and early design validation. This was followed by a detailed overview of the advanced chip design flow, highlighting the integration of RTL design, verification, synthesis, and physical implementation in modern SoC development. After the lunch break, the focus shifted to advanced ASIC design flows, covering architecture exploration, logic synthesis, timing optimization, and backend implementation through two comprehensive sessions for deeper technical insights.

Day- 4

The session opened with insights into next-generation CMOS devices, focusing on scaling challenges, emerging architectures, and innovations enhancing performance and energy efficiency. This was followed by a session on low-power design techniques, emphasizing dynamic voltage scaling, clock gating, and optimization strategies for minimizing power consumption in modern circuits. After the lunch break, the discussion continued with advanced ASIC design flow sessions, covering detailed aspects of physical design, timing closure, power planning, and design signoff processes for complex chip development.

Day-5

The session began with an exploration of the interrelationship between materials, devices, and packaging, highlighting innovations in semiconductor materials, thermal management, and advanced packaging techniques for improved device reliability and performance. This was followed by a session on high voltage chip design, focusing on design considerations, isolation techniques, and reliability challenges associated with high-voltage circuits. After the lunch break, the advanced ASIC design flow sessions continued, delving deeper into backend implementation, timing optimization, power integrity, and final design verification stages.

The FDP includes hands-on practices on the EDA tools with suitable IC examples.

Session's Industry Experts

- Prof. Pradeep Dixit, IIT Bombay
- Prof. Tarun Kumar Agarwal IIT, Gandhinagar
- Prof. Nihar Mohapatra, IIT Gandhinagar
- Prof. Bhaskar Mitra, IIT, Delhi
- Mr. Partha Vyas, Scaledge India Pvt. Ltd
- Prof. Anand Darji, SVNIT, Surat
- Prof. Rutu Parekh, DA-IICT, Gandhinagar
- Dr. Nikunj Tahilramani, Data Sentinel Inc
- Mr. Nirmit Patel, MicroCircuits Technologies,
- Mr. Akash Verma, MicroCircuits Technologies,
- Dr. R. A. Thakker, GTU

Registration Details:

- **Registration Link:** https://forms.gle/JYZ72dCSbq59A8t27
- **No Registration fees**
- **Last date of the Registration: 29th June 2025**
- Open for Faculty Members, Ph.D. Scholars of Electronics & Communication, Electrical Engineering, and Instrumentation & Control Disciplines
- **Mode of FDP:** Online