About GTU:

Gujarat Technological University (GTU) is a State University, NAAC A+ Accredited and premier academic and research institution which has driven new ways of thinking since its establishment in 2007. Today, GTU is an intellectual destination that draws inspired scholars to its campus, keeping GTU at the nexus of ideas that challenge and change the world. More than 350 institutes of Gujarat are affiliated with the GTU. The University caters to the fields of Engineering, Architecture, Management, Pharmacy and Computer Science. GTU has research and skilled based ecosystem in various emerging fields for the benefits of the stakeholders of the University.

GTU-SET Brief:

GTU School of Engineering and Technology (GTU-SET) established in 2017 by the GTU. It offers 2-years PG programs in Computer Engineering (Cyber Security), Internet of Things, Artificial Intelligence & Data Science, Civil Engineering (Structure Engineering), and 4 years UG programs in Computer Engineering and Electronics Communication Engineering. All programs are approved by the AICTE, New Delhi. The school offers full-time Ph.D. Programs in Computer Engineering, Electronics & Communication Engineering and Civil Engineering. The school is known to generate manpower with the state-of-the-art technical knowledge in the respective specialized fields. The school has CoEs in Blockchain and BOSCH Automation, AICTE Idea and ISEA sponsored laboratories and other state-of-art research laboratories.

FDP Details

Objectives of the FDP are:

- To familiarize participants with high-end semiconductor integrated circuit simulation tools: Cadence and Synopsis.
- To brief participants with basic and advanced features of circuit simulation and layout tools as well as device and process simulation tools.
- To make participants understand various complex analysis options available in the advanced simulation tools.
- To provide hands-on-session for better understanding and for the effective use of simulation tools for academic and research purposes.
- To contribute in training workforce for semiconductor technology mission of the state and nation.

Chief Patron

Dr. Rajul K. Gajjar, Hon'ble Vice Chancellor, GTU

Patron

Dr. K. N. Kher, Registrar, GTU

Convenor

Prof. Rajesh A. Thakker, Director, RDC, GTU
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GUJARAT TECHNOLOGICAL UNIVERSITY
AN INTERNATIONAL INNOVATIVE UNIVERSITY
(Accredited with A+ Grade by NAAC)
State Government University

Faculty Development Program

On

"Semiconductor Electronics Design Automation (EDA) Tools"

02-09-2024 to 06-09-2024

Jointly organized with

Entuple Technologies Pvt. Ltd, Bangalore
&
Eigen Technologies Pvt. Ltd. Guragaon

ENTUPLE TECHNOLOGIES

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Conducted by

Gujarat Technological University
School of Engineering and Technology,
Academic Block-5, GTU Campus,
Chandkheda, Ahmedabad, 382424

Session Details

Day-1: RTL to GDSII Flow using Synopsis EDA Tools

Overview of ASIC Design Flow, Introduction to Synopsys EDA Tools, RTL design simulation using VCS Synthesis of RTL using Design Compiler, Formal Verification using Formality, PnR stage using IC Compiler, Overview of Custom Design Flow, Schematic design & simulation using Custom Compiler, Layout Creation & verification in Custom Compiler.

Day-2: Design Simulation on TCAD Tool

Introduction to Sentaurus TCAD, Creation of Device Geometry using Sentaurus structure Editor, Exploring material Database, Process simulation using Sprocess, Extraction of Electrical Characteristics using Sdevice, Simulation Management and Parameter addition using SWB.

Day-3: IC Design Flow using Cadence EDA Tools

Introduction to Full Custom IC Design Flow, Cadence Solutions for Custom IC Design, MOSFET Characterization, Schematic Capture using Virtuoso Schematic Editor, Symbol Creation, Testbench Creation using Virtuoso Schematic Editor, Functional Simulation using Spectre, Delay Estimation, Power estimation, Monte-Carlo analysis, Layout Design using Virtuoso Layout Editor, Physical Verification which includes DRC & LVS, Parasitic Extraction using Quantus, Post Layout Simulation, Generation of GDSII.

Day- 4: IC Design Synthesis

Introduction to IC Physical Design Flow, Cadence EDA tools for PD Flow, Functional Simulation using Incisive tool, Coverage analysis using IMC tool, Introduction to TCL Scripting, RTL Synthesis using Genus Synthesis Solution. Physical Implementation using Innovus that includes Floor Planning, Power Planning, Placement, CTS, Routing, Timing Analysis, Power Analysis, Parasitic Extraction, Generation of GDSII with demonstrated by using COUNTER as an example.

Day-5: IC Design Analysis and DFT

Introduction to STA, Timing Analysis using Innovus, STA flow using TEMPUS tool, Introduction to Functional Verification, Functional Verification using Conformal LEC Tool, Pre & Post Synthesis Analysis, Introduction to DFT (Design For Test), Synthesis based on DFT using Modus tool, ATPG Based DFT, Introduction to Power Analysis, Power Analysis using VOLTUS, Basic flow using VOLTUS tool.

All session include hands-on practices on the EDA tools with suitable IC examples

Session's Industry Experts

- Mr. Vyom Sharma, Sr. Application Engineer, Eigen Technology Pvt. Ltd.
- Mr. Prashanth, Application Engineer-I, Eigne Technology Pvt. Ltd
- Mr. Johnson Pter, Manager, Entuple Technologies Pvt. Ltd., Pune
- Mr. Shivaprasad B. K., Execution Manager, Entuple Technologies Pvt. Ltd., Pune
- Mr. Swapnil Moon, Entuple Technologies Pvt. Ltd., Pune
- Ms. Soma Shekhar, Senior Engineer, Entuple Technologies Pvt. Ltd., Pune

Registration Details:

* Registration Link: https://forms.gle/NAZyRrjt5EkYZcGz7
* Registration fees for the faculty members, Ph.D. scholars, industry persons is Rs. 1,000/- including GST. All payment must be made online using given link: State Bank Collect (onlinesbi.sbi).
* **Last date of the Registration: 29th August, 2024**
* Open for Faculty Members, Ph.D. Scholars of Electronics & Communication, Electrical Engineering, and Instrumentation & Control and Allied Disciplines
* TA/DA and Accommodation will not be provided
* Registration kits, resource materials, breakfast, lunch and high-tea will be provided.
* **Steps for Payment of Fees**

  - State of Corporate/Institution: Gujarat
  - Type of Corporate/Institution: Educational Institutions
  - Educational Institutions Name: GUJARAT TECHNOLOGICAL UNIVERSITY
  - Select Payment Category: Registration Fees for Conference.
  - Fill your personal details. Conference Name as “FDP on Semiconductor EDA Tools” and pay the registration fees.
  - At the end, collect the Payment Ref. No. starting with DU”
  - Upload your payment receipt in registration form.